IN THE CLAIMS:

Presented below are a complete set of the claims. Please amend Claims 1, 7, 9-10, 12, 18-19, 32, and 38 as follows.

1. (Currently Amended)     A method of programming a memory comprising:

sending a command to a memory device, said command requesting said memory device to enter a fast program mode;

sending a first address to said memory device;

sending a first packet of data to said memory device, said first packet of data to be programmed at said first address;

sending a first write signal to said memory device, said first write signal to cause said first packet of data to be programmed at said first address;

sending a second packet of data to said memory device; and

sending a second write signal to said memory device, said second write signal to cause said second packet of data to be programmed at a second address, said second address generated by said memory device by incrementing said first address a predetermined amount.

2. (Original)     The method of claim 1 wherein said command is a fast program mode command.

3. (Original)     The method of claim 1 further comprising sending a confirmation of said command.

4. (Original)     The method of claim 1 wherein said first address is a starting address.

5. (Original)     The method of claim 1 wherein said memory device is a flash memory.

6. (Original)     The method of claim 1 further comprising sending a termination sequence to exit said program mode.

7. (Currently Amended)     The method of claim 6 8 wherein said termination sequence further comprises sending a data packet comprising all 1's to said memory device.

8. (Original)     The method of claim 6 wherein said termination sequence comprises sending a second address to said memory device, wherein second address is different from said first address.

9. (Currently Amended)     The method of claim 6 8 wherein said termination sequence

further comprises sending a ~~second address to said memory device, wherein said second address is the same as said first address~~ data packet comprising all 0's to said memory device.

10. (Currently Amended)    The method of claim 1 wherein said first address is sent to said memory device as long as said memory device is in said fast program mode.

11. (Original)    The method of claim 1 further comprising polling a pin on said memory device to determine a status.

12. (Currently Amended)    A method of writing data comprising:

receiving a command in a memory device, said command requesting said memory device to enter a fast program mode;

receiving a first address ~~in~~ at an address input of said memory device;

receiving a first packet of data, said first packet of data to be programmed at said first address;

receiving a write signal;

programming said first packet of data to said first address;

incrementing an internal program address from said first address to a second address, said second address sequential to said first address;

receiving a second packet of data;

receiving a second write signal; and

programming said second packet of data at said second address if an address at said address input is still said first address.

13. (Original)    The method of claim 12 wherein said command is a fast program mode command.

14. (Original)    The method of claim 12 further comprising receiving a confirmation of said command.

15. (Original)    The method of claim 12 wherein said first address is a starting address.

16. (Original)    The method of claim 12 wherein said memory device is a flash memory.

17. (Original)    The method of claim 12 further comprising receiving a termination sequence to exit said program mode.

18. (Currently Amended)    The method of claim ~~17~~ 19 wherein said termination sequence <u>further</u> comprises receiving a data packet comprising all 1's.

19. (Currently Amended)    The method of claim 17 wherein said termination sequence comprises receiving ~~an~~ <u>a</u> new address <u>at said address input of</u> ~~in~~ said memory device, wherein said new address is different from said first address.

20. (Original)    The method of claim 12 wherein said command is received in control logic within said memory device.

21. (Original)    The method of claim 20 wherein said control logic is a write state machine.

22. (Original)    The method of claim 20 wherein said command causes said control logic to program data at sequential addresses in said memory device.

23. (Original)    The method of claim 12 further comprising sending a status value from within said memory device to an output pin on said memory device.

24. (Cancelled).

25. (Cancelled).

26. (Cancelled).

27. (Cancelled).

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Currently Amended)    A machine readable medium having embodied thereon a computer program, the computer program being executable by a machine to perform a method comprising:

    sending a command to a memory device, said command requesting said memory
    device to enter a <u>fast</u> program mode;
    sending a first address to said memory device;
    sending a first packet of data to said memory device, said first packet of data to be
    programmed at said first address;
    sending a first write signal to said memory device<u>, said first write signal to cause</u>

said first packet of data to be programmed at said first address;

    sending a second packet of data to said memory device; and

    sending a second write signal to said memory device, said second write signal to cause said second packet of data to be programmed at a second address, said second address generated by said memory device by incrementing said first address a predetermined amount.

33. (Original)    The machine readable medium of claim 32 further comprising sending a confirmation of said command.

34. (Original)    The machine readable medium of claim 32 further comprising sending a termination sequence to exit said program mode.

35. (Cancelled).

36. (Cancelled)..

37. (Cancelled).

38. (Currently Amended)    A method comprising:

    receiving a command to enter a fast program mode to program a first piece of data at a first address;

    entering into a said fast program mode;

    programming said first piece of data at said first address in response to a write signal;

    checking whether termination of said fast program mode is indicated or if a second piece of data is to be written, wherein said checking further comprises detecting if an incoming address is different from said first address;

    exiting said fast program mode if said termination of said fast program mode is indicated, else incrementing said first address to a second address; and

    programming said second piece of data at said second address in response to another write signal.

39. (Previously Added)    The method of claim 38 further comprising receiving a confirmation command prior to entering said program mode.

40. (Previously Added)    The method of claim 39 further comprising issuing a status value to indicate a status for said programming of said first piece of data.

41. (Previously Added)     The method of claim 40 wherein indication said termination comprises:

    receiving an address unequal to said first address and a predefined data packet.

42. (Previously Added)     The method of claim 41 wherein said predefined data packet is comprised of all 1's.

43. (Previously Added)     The method of claim 41 wherein said predefined data packet is comprised of all 0's.